Remarks

Applicants respectfully request reconsideration of the present application in view of the following remarks. Claims 1-30, 32, and 34-37 remain pending in the current application.

I. Allowability of Claims 1-12 over the FIG. 1 Art, Phan, and Huang

Independent claim 1 is directed to a circuit for testing multiple memories and requires: "the resume input comprises a single input pin to the integrated circuit and the signal on the resume input to exit the idle state is asserted through a single channel between automated test equipment (ATE) and the integrated circuit" (emphasis added). For example, FIG. 3 of the present application shows a resume pin 108 that is a single input pin to the integrated circuit (IC) 82 and provides a single channel between ATE 22 and the IC 82.

By contrast, the FIG. 1 Art shows multiple input pins to the IC and thus multiple channels between the ATE and the IC. For example, the present application states at page 3, lines 17-19: "each BIST controller is coupled to a **separate "hold" pin**, such as **hold pins 30, 32**, on the IC 14" and "[t]he hold pins are coupled to the ATE 12, which **controls each hold pin individually**" (emphasis added). This configuration provides several disadvantages, such as the requirement of larger, more expensive ICs to accommodate the multitude of input pins as well as larger, more expensive ATEs to accommodate the multitude of channels.

Phan does not cure the deficiencies of the FIG. 1 Art. For example, Phan is understood to disclose in FIG. 2 an IC and an ATE 160 having **multiple channels in-between** (e.g., FLARESCAN_OUT, FUSE_PROGRAM, FUSESCAN_IN_CLK, and FLARESCAN_IN_CLK). Furthermore, Phan is understood to describe no input resembling a resume input. The inputs described (e.g., signals MEMORY ADDRESS, MEMORY CONTROL, and MEMORY DATA_IN to BIST 102 in FIG. 1) represent inputs other than a resume input, such as memory address bus signals, data bus signals, and control signals.

Huang also does not cure the deficiencies of the FIG. 1 Art. For example, Huang is understood to describe nothing relating to an ATE, much less channels between an ATE and an IC. Furthermore, Huang describes a BIST controller 22 (see FIG. 1) having multiple inputs, but none of the inputs is understood to be anything resembling a resume input. The inputs described in Huang are understood to represent other types of inputs (e.g., state transitions).

The FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single input pin to the integrated circuit and a single channel between automated test equipment (ATE) and the integrated circuit, as required by independent claim 1. Therefore, independent claim 1 and the corresponding dependent claims should be allowable over the cited art.

Dependent claims 2-12 depend directly or indirectly from independent claim 1 and are allowable for at least the reasons recited above in support of their parent claim 1. They are also independently patentable.

II. Allowability of Claims 13-18 over the FIG. 1 Art, Phan, and Huang

Independent claim 13 is directed to a circuit for testing multiple memories and requires: "automated test equipment (ATE), wherein the ATE receives the synchronization output through a single channel between the ATE and the integrated circuit" (emphasis added).

The FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single channel between the ATE and the integrated circuit, as required by independent claim 13. Therefore, independent claim 13 and the corresponding dependent claims should be allowable over the cited art.

Dependent claims 14-18 depend directly or indirectly from independent claim 13 and are allowable for at least the reasons recited above in support of their parent claim 13. They are also independently patentable.

III. Allowability of Claims 19-29 over the FIG. 1 Art, Phan, and Huang

Independent claim 19 is directed to a method of testing memory and requires: "wherein the synchronization signal is asserted through a single channel to automated test equipment (ATE)" (emphasis added).

The FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single channel to automated test equipment (ATE), as required by independent claim 19. Therefore, independent claim 19 and the corresponding dependent claims should be allowable over the cited art.

Dependent claims 20-29 depend directly or indirectly from independent claim 19 and are allowable for at least the reasons recited above in support of their parent claim 19. They are also independently patentable.

IV. Allowability of Claims 30, 32, and 37 over the FIG. 1 Art, Phan, and Huang

Independent claim 30 is directed to a method of testing memories and requires: "the resume input comprises a single input pin to the integrated circuit and a signal on the resume input is asserted through a single channel between automated test equipment (ATE) and the integrated circuit" (emphasis added).

The FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single input pin to the integrated circuit and a single channel between automated test equipment (ATE) and the integrated circuit, as required by independent claim 30. Therefore, independent claim 30 and the corresponding dependent claims should be allowable over the cited art.

Dependent claims 32 and 37 depend directly or indirectly from independent claim 30 and are allowable for at least the reasons recited above in support of their parent claim 30. They are also independently patentable.

V. Allowability of Claims 34-36 over the FIG. 1 Art, Phan, and Huang

Independent claim 34 is directed to a computer readable medium on which is stored a software tool containing instructions for performing a method that requires: "the resume input comprises a single input pin to an integrated circuit comprising the BIST controller and a signal on the resume input is asserted through a single channel between automated test equipment (ATE) and the integrated circuit" (emphasis added).

The FIG. 1 Art, Phan, and Huang, alone or in combination, fail to teach or suggest a single input pin to an integrated circuit and a single channel between automated test equipment (ATE) and the integrated circuit, as required by independent claim 34. Therefore, independent claim 34 and the corresponding dependent claims should be allowable over the cited art.

Dependent claims 35 and 36 depend directly or indirectly from independent claim 34 and are allowable for at least the reasons recited above in support of their parent claim 34. They are also independently patentable.

VI. Conclusion

Applicants respectfully submit that the present application is in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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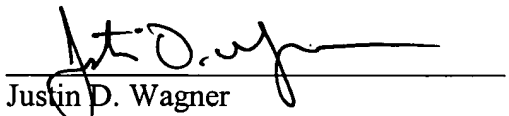
By 

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